REMARKS

Claims 1-9, 11-18, and 21-34 are pending in the application.

The Examiner rejects claims 15 and 16 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that Applicants regards as their invention.

The Examiner rejects claim 15 under 35 U.S.C. § 102(b) as being anticipated by the acknowledged prior art of Figure 2 ("APA").

The Examiner rejects claims 15, 16, 29, and 30 under 35 U.S.C. § 102(b), as being anticipated by Klein, U.S. Patent No. 6,349,051, ("Klein").

The Examiner rejects claims 1, 4, 5, 12-14, 25, 26, and 32-34 under 35 U.S.C. § 103(a) as being unpatentable over Klein in view of APA.

Applicants amend claims 1, 12, 15, 25 and 29, and add claims 34-41.

Claims 1-9, 11-18, and 21-41 remain in the application.

Applicants add no new matter and request reconsideration.

Claims Allowed

Applicants thank Examiner Dang for the allowance of claims 9, 11, 17, 18, 21-24, and 31.

Claim Rejections – 35 U.S.C. § 112

The Examiner rejects claims 15 and 16 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that Applicants regards as their invention.

Applicants amend claim 15 to obviate the Examiner's rejection. For further clarity Applicants respectfully direct the Examiner to specific portions of specification. See, e.g., paragraphs beginning on page 8, line 23, page 9, line 7, and page 12, line 18, and Figures 4, 5, and 7. For instance, the specification recites, "the memory controller embeds, within its address/command signals, information that *identifies the memory unit*, device, or rank *selected for a particular read or write operation.* For instance, with six ranks, six *unique read commands* (READ*n*, where *n* identifies a rank between 0 and 5, inclusive) are defined," and "[t]he address/command decoder on *each memory device decodes each read* or write *command issued by the memory controller*, regardless of whether chip select has been

asserted for that device." See Specification, page 8, line 23 – page 9, line 2, page 9, lines 7-10, and page 12, lines 18-20. Thus, the above-recited references to the specification, when read in conjunction with their corresponding figures, clearly illustrate that a READ command signal(s) uniquely identifies which memory unit is to perform the read operation, and that the memory unit to perform the operation is identified to all of the memory units. Applicant requests that in view of the above references of the specification and the claim amendment that the rejection be withdrawn.

Claim Rejections – 35 U.S.C. § 102 and § 103

The Examiner rejects claim 15 under 35 U.S.C. § 102(b) as being anticipated by APA. Applicants respectfully traverse the Examiner's rejection.

Amended claim 15 recites *the READ command signals identify, to each memory unit, which memory unit of the multiple memory units is to perform a data read operation.* The Examiner alleges the APA discloses the recited limitation. APA's command signals, however, "instruct a memory device as to what *type of operation is to be performed*, e.g., read, write, refresh," not which memory unit of the multiple memory units is to perform the operation. See Specification, page 1, line 18 – page 2, line 8. Since APA's command signals do not disclose identifying the memory unit currently being addressed, the APA, therefore, does not anticipate claim 15 or its corresponding dependent claim.

The Examiner rejects claims 15, 16, 29, and 30 under 35 U.S.C. § 102(b), as being anticipated by Klein. The Examiner rejects claims 1, 4, 5, 12-14, 25, 26, and 32-34 under 35 U.S.C. § 103(a) as being unpatentable over Klein in view of APA. Applicants respectfully traverse the Examiner's rejection.

Amended claim 1 recites *termination circuitry to absorb signals on the second drop responsive to the on state*. Claims 12, 25, and 29 recite a similar limitation. The Examiner alleges Klein's transfer gates 64 disclose the recited termination circuitry. Transfer gates 64, however, reduce parasitic capacitances by removing a load condition on data bus 70, specifically by isolating a bus segment and a corresponding memory module 76 from data bus 70, not *absorbing the signals on the second drop* as the claim requires. See, e.g., Figures 2 and 6; Klein, col. 3, lines 16-22 and 46-50. Since transfer gates 64 do not absorb signals on the second drop, Klein, therefore, does not anticipate claim 1, or claims 12, 25 and 29, and their corresponding dependent claims.

Claim 15 recites *an address/command generator to generate address and command signals for multiple memory units, including READ command signals, wherein the READ command signals identify, to each memory unit, which memory unit of the multiple memory units is to perform a data read operation.* Claim 25 recites a similar limitation.

The Examiner alleges Klein's control signals 68 and memory module 60 disclose the recited READ command signals and memory unit, respectively. Control signals 68, however are conventional control signals, such as "row address strobe (RAS), column address strobe (CAS) and write enable (WE) familiar to those in the art," which do not identify, to each memory module 60, which memory module 60 among a plurality of memory modules 35 is to perform the recited data read operation. Klein, col. 5, ll. 52-55; col. 6, ll. 4-7 and 31-51; Figures 3 and 7. The Examiner states "it is clear from Klein that each READ command signal must identify the memory unit because the location of memory device has already been specified by the address signals. Without identifying the addressed memory unit, a READ operation simply cannot be performed." Contrary to the Examiner's assertions, Klein selects a memory module 60 to perform read and write operations by providing a chip select signal to the selected memory module 60. Klein, col. 6, lines 37-39; Figure 10. Klein, however, does not disclose *identifying*, to each memory module 60, which memory module receives the chip select signal and thus performs a read or write operation. Since Klein does not identify to each memory module, which memory module is to perform a data read operation, Klein, therefore, does not anticipate claim 15, or claim 25, and their corresponding dependent claims.

Claim 29 recites *the register value including fields to indicate, to the memory unit, state conditions under which the memory unit should enable and/or disable a data bus line termination circuit on the memory unit.* Klein does not teach or suggest control signals 68, such as "row address strobe (RAS), column address strobe (CAS) and write enable (WE) familiar to those in the art," including the recited fields. See, Specification, page 9, line 12 – page 10, line 1; Klein, col. 5, ll. 52-55. Klein, therefore, does not anticipate claim 29 or its corresponding dependent claims.

Added Claims 34-41

Applicants add claims 34-41 as rewritten claims 2, 6, and 27 in independent form, and their corresponding dependent claims.

CONCLUSION

For the foregoing reasons, the Applicants request reconsideration and allowance of all claims as amended. The Applicants encourage the Examiner to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

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Respectfully submitted,

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